REMARKS

Claims 1 and 3-14 are pending in the above-identified application. Claims 1, 3, 4, 6, 8, 10, 11, and 13 are independent.

Information Disclosure Statement

The Information Disclosure Statements filed April 19, 2000, December 24, 2002, and December 30, 2002 have not been acknowledged by the Examiner as to consideration of the reference cited therein. **Therein, the Examiner is respectfully requested to provide Applicant with an initialed PTO-1449 Form, indicating consideration of the Information Disclosure Statements submitted April 19, 2000, December 24, 2002, and December 30, 2002.**

Claim Rejection – 35 U.S.C. 102

Claims 1-4, 6, 8-11, and 13 have been rejected under 35 U.S.C. 102(b) as being clearly anticipated by Omichi et al. (JP 01-223586, hereinafter Omichi). Applicants respectfully traverse this rejection.

The present invention is directed to a microcomputer having built-in nonvolatile memory and check system thereof. The system is capable of simultaneously testing a large number of IC cards automatically, over various kinds of tests. Also, the system requires a low amount of communication between the microcomputer and an external testing apparatus.

In particular, the microcomputer of the present invention includes a boot ROM that enables automatic control of the testing process. The boot ROM contains a program to operate the communication circuit 14. Upon receiving a command from an external communication device, the program sets the conditions necessary for transfer and performs transfer of the test program from the external communication device to the RAM. The program runs the test program and sends the test results to the external communication device (see Figure 3). As mentioned above, this enables automatic control of the testing process in the microcomputer and reduces communication with the external communication device.

The Office Action alleges that Omichi's ROM teaches the claimed boot ROM (with respect to original claim 2). Applicants submit that Omichi does appear to disclose that control programs or basic processing programs or operation programs of the MPU 8 are stored in a ROM 4 (page 6 of the translation). It discloses that functional elements of the MPU 8, including a test program writing means 6 and test program implementation means 7, may be realized by programs implemented in the ROM 4 (page 7 of the translation). The test program writing means 6 receives data existing in the data block transmitted from the testing device via the identification means 2 and sequentially writes the data into an operation test program area 51 (page 8 of the translation). The operation test program written in the RAM is implemented by the test program implementation means 7 (page 9 of the translation). Mode identification information is stored in an identification means 2.

Omichi also does appear to disclose operations of transmitting a data block to the identification means 2. If it is determined that the mode identification information of the data block shows storage of the operation test program, the test program writing means is started by the identification means 2. The test program writing means receives the data existing in the data block and sequentially writes the data into an operation test program area 51. The operation test program written in the RAM is implemented by the test program implementation means 7 (page 9 of the translation). Upon completion of a test item, if operation confirmation is not finished, another instruction is received from the testing device and processing of the next test item is performed.

In summary, the ROM in Omichi may store the programs run by the MPU, and the programs may be started by data existing in an identification means. For example, the test program writing means 6 receives the data existing in the data block in the identification means and sequentially writes the data into an operation test program area 51. Also, based on the test program implementation means 7 an instruction for each test item of the test operation is transferred from the test device.

Applicants submit that Omichi does not teach or suggest at least the claimed boot ROM having the control program recited in the claim. In particular, if Omichi's ROM stores the test program writing means, it controls transfer of a data block from the identification means. In the claimed invention, on the other hand, the boot ROM comprises a control program that controls communications in the microcomputer including receiving of the test program

from an external check system and running the test program on the RAM. In other words, Omichi's ROM is not a boot ROM according to the context of the claimed invention (i.e., not a boot ROM, *per se*).

Accordingly, Applicants submit that Omichi fails to teach or suggest each and every claimed element of claims 1-4, 6, 8-11, and 13.

Claim Rejection – 35 U.S.C. 103

Claims 5, 7, 12, and 14 have been rejected under 35 U.S.C. 103 as being unpatentable over Omichi in view of Lin et al. (U.S. Patent 5,818,848, hereinafter Lin). Applicants respectfully traverse this rejection.

With respect to claims 5, 7, 12, and 14, a plurality of external communication devices enables connection of a control computer and a plurality of microcomputers, such that the plurality of microcomputers can be tested simultaneously (Specification: page 16, lines 22 to 25). In addition, by having a plurality of external communication devices, less work load is on the control computer in controlling testing of the plurality of microcomputers. In an example embodiment, a control computer 30 can be connected to a large number of external communication devices 20 for simultaneous testing of a number of nonvolatile memories of microcomputers 10.

Specifically, the claims are directed to a check system of a microcomputer having a built-in nonvolatile memory comprising at least one external communication device connected to the microcomputer, and a control computer, connected to the plurality of external communication devices. Some claims are alternatively directed to testing of IC cards.

The Office Action alleges that Omichi teaches all claimed elements except for the control computer. The Office Action instead relies on Lin for making up for the deficiency of Omichi. In particular, the Office Action alleges that Lin's system comprising a control computer connected to a plurality of integrated circuits of a test board teaches the claimed control computer connected to a plurality of external communication devices, for controlling check-up of a plurality of microcomputers. However, Applicants submit that Lin does not teach a plurality of external communication devices for controlling the plurality of microcomputers. Rather, the processing load of controlling the testing of the integrated circuits 00, 01, 10, 11, 20, etc. is on the test control processor 100. Thus, at least for this reason, Applicants submit that the rejection fails to establish prima facie obviousness.

CONCLUSION

In view of the above amendments and remarks, reconsideration of the various rejections and allowance of claims 1 and 3-14 is respectfully requested.

Should the Examiner have any questions concerning this application, the Examiner is invited to contact Robert W. Downs (Reg. No. 48,222) at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully Submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claim 2 has been canceled.

The claims have been amended as follows:

1. (Amended) A microcomputer having a built-in nonvolatile memory including:

a communication circuit for receiving a test program for a nonvolatile memory from an external check system; [and]

a RAM on which said test program is run; and

a boot ROM in which a control program for enabling receiving of said test program through said communication circuit and running of said test program on said RAM.

4. (Amended) A check system of a microcomputer having a built-in nonvolatile memory furnished with:

at least one external communication device connected to said microcomputer in such a manner so as to allow a communication in a one-to-one correspondence,

each external communication device including,

a storage device having stored a test program for a built-in nonvolatile memory in said microcomputer, and

a communication microcomputer for sending said test program to said microcomputer,

wherein said microcomputer includes a boot ROM in which a control program for enabling receiving of said test program through a communication circuit and running of the test program on a RAM.

6. (Amended) A check system of a microcomputer having a built-in nonvolatile memory furnished with an external communication device including:

a storage device having stored a test program for said microcomputer having a built-in nonvolatile memory;

a communication control circuit for controlling a communication with said microcomputer; and

a communication microcomputer for sending said test program to said microcomputer when checking the built-in nonvolatile memory therein,

wherein said microcomputer includes a boot ROM in which a control program for enabling receiving of said test program through a communication circuit and running of the test program on a RAM.

8. (Amended) An IC card packing a microcomputer having a built-in nonvolatile memory including:

a communication circuit for receiving a test program for a nonvolatile memory from an eternal check system; [and]

a RAM on which said test program is run, and

a boot ROM in which a control program for enabling receiving of said test program through said communication circuit and running of said test program on said RAM.

11. (Amended) A check system of an IC card packing a microcomputer having a built-in nonvolatile memory furnished with:

at least one external communication device connected to said microcomputer packed in said IC card in such a manner so as to allow a communication in a one-to-one correspondence,

each external communication device including,

a storage device having stored a test program for a built-in nonvolatile memory in said microcomputer, and

a communication microcomputer for sending said test program to said IC card,

wherein said microcomputer includes a boot ROM in which a control program for enabling receiving of said test program through a communication circuit and running of the test program on a RAM.

13. (Amended) A check system of an IC card packing a microcomputer having a built-in nonvolatile memory furnished with an external communication device including:

a storage device having stored a test program for a built-in nonvolatile memory in said microcomputer packed in said IC card;

a communication control circuit for controlling a communication with said IC card; and

a communication microcomputer for sending said test program to said IC card when checking said built-in nonvolatile memory,

wherein said microcomputer includes a boot ROM in which a control program for enabling receiving of said test program through a communication circuit and running of the test program on a RAM.